

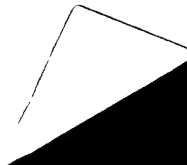
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When the driving circuit is incorporated in the image display apparatus, the increase of the display gradation number of the image display apparatus (namely, the bit number of data) will result in the expansion of the region in which the driving circuit is formed in accordance with the increase of the number of the data lines. The increase of the region in which the driving circuit is formed in accordance with the

When the driving circuit is incorporated in the image display apparatus, the increase of the display gradation number of the image display apparatus (namely, the bit number of data) will result in the expansion of the region in which the driving circuit is formed in accordance with the increase of the number of the data lines. The increase of the region in which the driving circuit is formed in accordance with the

increase of the display gradation number, however,
results in the expansion of the non-display region.
Thus, the area in which the driving circuit is formed
must be limited. For example, in order to attain the
5 image display apparatus having the definition of 200
pixels/inch with the pixels of the vertical color
stripes, the interval of the signal lines is required
to be $2.54 \text{ mm} \div 200 \div 3 \text{ (colors)} \cong 42 \text{ } \mu\text{m}$. The circuit
for driving one signal line must be disposed in this
10 interval.

However, when the image display apparatus
having the definition of 200 pixels/inch is tried to be
constructed according to the conventional construction,
the interval between the signal lines cannot be
15 achieved as required because of the large number of the
wiring lines.

That is, the prior image display apparatus is
constructed in the following manner in order to
transfer the 6-bit binary data to the DA converter.
20 The data bus and the one latch are connected through
the six lines, the one latch and the other latch are
connected through the six lines, and the other latch
and the DA converter are connected through the six
lines. In addition, the image display apparatus uses
25 two types of metals (namely, the gate metal used for
the gate electrode of the thin film transistor
(hereinafter, referred to as "TFT") and the wiring
metal connected to the source and drain electrodes of

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Therefore, the six wiring lines (longitudinal lines) for connecting the data bus and the DA converter between which the two latches are provided, and the group of the lateral gradation voltage lines arranged to intersect the longitudinal lines at the DA converter are formed as two separate wiring layers. As a result, the six longitudinal lines cannot be overlapped each other, so that they are obliged to be formed in parallel. Accordingly, when the space and the wiring line are selected to be $4\text{ }\mu\text{m}$ and $4\text{ }\mu\text{m}$ according to the layout rule, the six wiring lines need the total width of $(4+4) \times 6$ (lines) = $48\text{ }\mu\text{m}$, which thus exceeds the required line width of $42\text{ }\mu\text{m}$.

Moreover, the number of the TFTs is greatly affected by the increase of the gradation number. When the bit number of data is k , the DA converter alone needs the arrangement of the TFTs, the number of which is $k \times 2^k$ (e.g., 384 when k is 6). In addition, in order to provide two k -bit latches, it is necessary to use the layout rule of 1 μm or below, which is actually impractical.

Also, the power consumption of the driving circuit incorporated in the image display apparatus is required to be as small as possible. That is, the power consumption of the image display apparatus

5 functions to transmit the input data from the outside
to the latches. The data bus is one of the wiring
lines having the fast data transmission rate and the
large power consumption. The power consumption of this
data bus is proportional to the wiring capacitance, the
10 number of the data changes, and the square of the
signal voltage. Therefore, the power consumption of
the data bus can be effectively reduced by decreasing
the wiring capacitance, the number of the data changes,
and the signal voltage. The wiring intersection
15 capacitance of the wiring capacitance of the data bus
is the great part.

20 line are necessary as the wiring intersections of the data buses in order for the data from the data bus to be taken out at the one latch as in the prior art.

25 to "0"), when "k" is assumed to be the number of the wiring lines of the data bus, the average data changes per data is $k/2$ (3 when six bits are used), and the maximum number of the data changes is k (6 when six

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image data;
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5 voltage from the specified gradation voltage line to a
specified signal line.

The following elements can be added when the above image display apparatus is constructed.

(1) The decoder means is divided into a plurality
10 of decoders which are arranged to oppose each other.

(2) A plurality of switch drive lines for transmitting the switch drive signals are connected to the decoder means; a plurality of trigger lines for transmitting the trigger signals are connected to the trigger signal output means; and output lines for transmitting the specified gradation voltage to the specified signal line are connected to the plurality of switch means.

(3) The plurality of switch drive lines and the group of gradation voltage lines are arranged to intersect the plurality of trigger lines and the output lines.

(4) The group of gradation voltage lines are arranged in parallel along the plurality of switch drive lines.

(5) The switch drive lines is arranged in parallel with one gradation voltage line of the group of gradation voltage lines.

5 (7) The group of gradation voltage lines and the
plurality of switch drive lines are formed as a same
wiring layer.

10 (9) Distribution means for distributing output
voltage from the output lines to the plurality of
signal lines is provided between the output lines and
the plurality of signal lines.

(11) When n is a display gradation number, a wiring number of the group of gradation voltage lines is in a range from n to $2n$.

(13) The decoder means is disposed on a surface of
25 the substrate or on a periphery of the substrate.

(14) The image display means, the group of gradation voltage lines, the plurality of switch means, the decoder means and the trigger signal output means

(15) The trigger signal output means is formed using a shift register circuit.

(16) Each of the plurality of switch means includes: a first thin film transistor which becomes conductive by being inputted the trigger signal to transmit the switch drive signal; and a second thin film transistor which becomes conductive by the switch drive signal produced from the first thin film transistor to transmit a gradation voltage to the output line.

(17) Each of the plurality of switch means includes a condenser for holding the switch drive signal produced from the first thin film transistor.

(18) The condenser is an electrostatic capacity formed by overlapping any one gradation voltage line of the group of gradation voltage lines and an electrode formed in a wiring layer different from the group of gradation voltage lines.

(19) Each of the plurality of switch means includes memory means for storing the switch drive signal produced from the first thin film transistor as at least one-bit information.

(20) The plurality of switch means are disposed in regions near intersections at which the switch drive lines and the trigger lines are intersected each other, respectively.

(21) The first thin film transistor and the second

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gradation voltage lines.

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(27) Each of the pixel includes a liquid crystal interposed between a pair of substrates including a transparent insulating substrate; and a light

(28) Each of the pixels includes a light emitting film formed on an insulating substrate; and a light emission intensity of the light emitting film is changed in accordance with a voltage from the switch element connected to the pixel.

(29) It further includes scanning means for

(30) When the image display apparatus is driven, a drive frequency at which the switch drive signals are supplied from the decoder means to the plurality of switch drive lines is set to twice or more as high as a drive frequency at which the trigger signals are supplied from the trigger signal output means.

(31) The number of simultaneous data switching for a gradation data inputted to the decoder means is two or less; and the decoder means sequentially produces switch drive signals for selecting one single switch drive line in accordance with the gradation data.

According to the above means, the decode means is constructed to have the digital/analogue conversion function for converting the gradation data to the analogue signal, and the function for selecting the signal line. A specified gradation voltage line is selected in accordance with the switch drive signal

5 the signal line drive circuits provided in the non-
display region can be reduced to be smaller than th
display region in which the high-definition multi-t
images are displayed.

In addition, since the decoder means is used
10 to select one single gradation voltage line, the number
of the switch drive lines on which data is changed is
maximum "2", so that the number of times that data is
changed is reduced. Thereby, even if the capacitance
between the wiring lines is charged or discharged each
15 time data is changed, the power consumption can be
lowered by the reduction of the number of times that
data is changed.

Moreover, when the multi-tone images are displayed, the intersection wiring lines (i.e., the intersection wiring line capacitance) can be reduced, so that the power consumption on the switch drive lines for transmitting the fast signals can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the construction
25 of a main part of an image display apparatus according
to an embodiment of the present invention;

Fig. 2 is a diagram for explaining a method

of generating gradation voltages from a plurality of voltage sources;

Fig. 3 is a diagram for explaining a method of generating the gradation voltages using a ladder resistor;

Fig. 4 is a circuit diagram showing another example of a switch circuit used in an image display apparatus according to the present invention;

Fig. 5 is a block diagram of a decoder used in an image display apparatus according to the present invention;

Fig. 6 is a diagram for explaining the logic of the decoder shown in Fig. 5;

Fig. 7 is a block diagram of an arrangement where the decoder shown in Fig. 1 is used as an external IC;

Fig. 8 is a circuit diagram of a shift register in an image display apparatus according to the present invention;

Figs. 9A-9C are diagrams for explaining constitution components of the shift register shown in Fig. 8;

Fig. 10 is a time chart for explaining the operation of the shift register shown in Fig. 8;

Fig. 11 is a circuit diagram of another example of the switch circuit used in the image display apparatus according to the present invention;

Fig. 12 is a diagram showing the structure of

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Fig. 13 is a diagram showing the structure of

Fig. 14 is a time chart for explaining the operation of an image display apparatus according to the present invention;

15 Fig. 16 is a diagram for explaining the logic
of the decoder when an image display apparatus
according to the present invention is constructed as a
liquid crystal display apparatus;

Fig. 17 is a diagram for explaining another
20 alternation method of when an image display apparatus
according to the present invention is constructed as a
liquid crystal display apparatus;

Fig. 18 is a graph for explaining the relation between the gradation and the voltage when an image display apparatus according to the present invention is constructed as a liquid crystal display apparatus;

Fig. 19 is a diagram for explaining the logic

Fig. 20 is a diagram showing the circuit
5 layout of a DA converter in an image display apparatus
according to the present invention;

10 Fig. 22 is a diagram for explaining the level
conversion operation of a switch circuit used in the
apparatus shown in Fig. 21;

15 Fig. 24 is a diagram for explaining the
circuit layout of the DA converter in the apparatus
shown in Fig. 21;

Fig. 25 is a diagram showing the construction
of a main part of the third embodiment of an image
20 display apparatus according to the present invention;

Fig. 27 is a circuit diagram showing a distribution circuit in an image display apparatus according to the present invention.

One embodiment of the present invention will

insulating substrate 1, there are formed a shift register 2, a decoder 3, a DA converter 4, a scanning circuit 5 and a display region 6. This display region 6 is formed as a region for displaying the high-definition multi-tone image. A plurality of signal lines S1-S6 and a plurality of scanning lines G1 and G2 are disposed in the display region 6 in a matrix shape. Pixel TFTs 7 functioning as switch elements, and pixels 8 are formed in the respective regions near the intersections of the signal lines and the scanning lines. The gate electrodes of the pixel TFTs 7 are connected to the scanning lines G1 and G2, their source electrodes are connected to the signal lines S1-S6, and their drain electrodes are connected to the pixels 8 as illustrated.

20 In this embodiment, six signal lines, two scanning lines, 6×2 pixel TFTs 7 and 6×2 pixels 8 are shown for the sake of simple explanation. However, these numbers are actually dependent on the number of the pixels 8. For example, when the display amount
25 information of the image display apparatus corresponds to the color VGA, each of the numbers of the pixels 8 and the pixel TFTs 7 are $640 \times 480 \times 3$ (red, green and blue). Thus, the numbers of the signal lines and the



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5 (nonconductive) when the low voltage is applied to the
condenser Cm.

10 gradation voltage line LV1 in response to the data
(switch drive signal) from the switch drive line.
Then, the switch means supplies the gradation voltage
V1 from the specified gradation voltage line LV1 to the
signal line S1 via the output line X1. The switch
15 circuits arranged in a matrix shape at all the
intersections of the output lines X1-X6 and the switch
drive lines D1-1 to Dn-1 and D1-2 to Dn-2 are similarly
constructed as mentioned above.

20 means which produces the switch drive signal for selecting any gradation voltage line according to the digital multi-tone image data (n-bit image data, for example, image data of six-bit 64 gradations). The decoder 3 in this embodiment has two separate data

25 lines Data-1 and Data-2 from which the image data is supplied so that data of "1" (switch drive signal) can be fed to two switch drive lines according to the multi-tone image data.

In other words, the decoder 3 has two decoders 11 and 12 as shown in Fig. 5. When the high-gradation image data are supplied from the data lines Data-1 and Data-2 to the input terminals A-1 and A-2, the decoders 11 and 12 produce "1" signal (switch drive signal) at only a single output terminal of each of two separate output terminals Y1-1 to Yn-1 and Y1-2 to Yn-2, and "0" signal at the other output terminals according to the logic shown in Fig. 6.

Here, "1" means the high voltage, and "0" means the low voltage. The input in is binary data. Although the data inputting to the input in is expressed by 1 through n for the sake of better understanding, it may be any n different values such as figures of 0 through (n-1). In addition, although two separate input terminals A-1 and A-2 are provided as the input terminals of the decoder 3, a separator may be provided before the input terminals of the decoders 11 and 12 so that a single input terminal can be effective.

Although the decoder 3 is provided on one side, the decoders 11 and 12 may be provided on both sides of the DA converter 4, respectively. In addition, the decoder 3 may be provided as an external IC 23 on the outside of the insulating substrate 1 so that the external IC 23 can be connected via a flexible cable (FPC) 24 to the insulating substrate 1 as shown in Fig. 7. Also, the external IC 23 may be mounted

directly on the surface of the insulating substrate 1.

The shift register 2 as trigger signal output means for sequentially producing the trigger signals in synchronism with the image data is constructed using 5 inverters, clocked inverters and AND gates, as shown in Fig. 8, for example. The inverters, the clocked inverters and the AND gates can be constructed by circuits using TFTs, as shown in Figs. 9A-9C, respectively. The shift register 2 responds to a clock 10 CK, a reverse-phase clock CKN and a start pulse ST to sequentially generate the trigger signals (trigger pulses) q1, q2 and q3 from the AND gates. Although the trigger pulses q1-q3 are produced in turn from the shift register 2, the order in which the trigger pulses 15 are generated depends on the relation between the input data and the signal lines, and it is thus particularly not limited.

The scanning circuit 5 is constructed using the similar circuits as is the shift register 2, for 20 example, and is constructed as scanning means for sequentially producing the scanning pulse signals on the scanning lines G1 and G2.

The n-channel TFTs are used for the switch circuits SW of the DA converter 4 as described above. 25 However, the mixture of the switch circuits SW using the n-channel TFTs, and the switch circuits SWp using the p-channel TFTs can be used to construct the DA converter 4, as shown in Fig. 11. In other words, when

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the gradation voltage of the gradation voltage line LV_i is relatively lower than the signal voltage of the switch drive line Di , the signal source voltage to the switch drive lines can be reduced by using the n-channel TFT tr_2 . On the other hand, when the gradation voltage of the gradation voltage LV_j is relatively higher than the signal voltage of the switch drive line Dj , the signal source voltage to the switch drive lines can be reduced by using the p-channel TFTs tr_{2p} . In this case, when the switch circuits SW_p using the p-channel TFTs are connected to the decoder 3, an inverter 25 can be provided between the decoder 3 and the switch circuit SW_p in order to invert the output logic of the decoder 3, or the structure for inverting the logic can be employed within the decoder 3.

When the image display apparatus is used as a liquid crystal display apparatus, the pixels 8 provided in the display region 6 can be each constructed by a condenser 27 that holds the voltage sampled by the pixel TFT 7, and a liquid crystal layer 29 interposed between the insulating substrate 1 and the opposed substrate (transparent substrate), as shown in Fig. 12. The condenser 27 has its one end connected to a ground line 28 so that the voltage sampled by the pixel TFT 7 can be stably held for one-frame period. The liquid crystal layer 29 has its one end connected to a common electrode 30 so that the difference voltage between the voltage held on the condenser 27 and a voltage V_c

applied on the common electrode 30 can be applied across the liquid crystal layer 29. Thereby, it is possible to change the light transmission factor of the liquid crystal layer (liquid crystal) 29 to display the
5 image.

When the image display apparatus is used as a self-emitting type display apparatus, the pixels 8 can be each constructed by a condenser 31 for holding the voltage sampled by the pixel TFT 7, a voltage/current
10 conversion circuit 32 for converting the voltage sampled by the pixel TFT 7 into the current, and a light-emitting layer 33, as shown in Fig. 13. The one ends of the condenser 31 and the light-emitting layer 33 are connected to a ground line 34, and the voltage
15 from a power source line 35 is applied to the voltage/current conversion circuit 32. When the external voltage is applied between the power source line 35 and the ground line 34, and the sampled voltage is held on the condenser 31, the light emission
20 intensity of the light emitting layer 33 can be changed in accordance with the held voltage, thus displaying the image.

When the image is displayed on the display region 6, the circuits of the image display apparatus
25 operate as shown in Fig. 14. First, as the multi-tone image data, the odd-numbered image data is applied to the data line Data-1 of the decoder 3, and the even-numbered image data is applied to the data line Data-2

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of the decoder 3. For example, when a row of image data #1-#6, which are displayed on the display region 6, are [2, 3, 4, 2, 1, n] from left to right in turn, the image data [2, 4, 1] is fed to the data line Data-1, and the image data [3, 2, n] is fed to the data line Data-2. When the image data is decoded by the decoder 3, one of the switch drive lines D1-1 to Dn-1 is turned "1", and one of the switch drive lines D1-2 to Dn-2 is turned "1", as the switch drive lines selected by the image data. The shift register 2, in synchronism with the input of this image data, outputs the trigger pulses on the trigger lines Q1-Q3 in turn. When the trigger pulses are sequentially output, the n-channel TFTs tr1 connected to the trigger lines Q1-Q3 are turned ON, thus sequentially sampling the data on the switch drive lines. Of the switch circuits SW connected to the trigger lines Q1-Q3, the switch circuits SW with data of "1" produced on the switch drive lines stores the data of "1" corresponding to the image data. Further, the switch circuits SW with data of "0" produced on the switch drive lines stores data of "0". These stored data are held until these data are sampled again. During this interval, the TFTs tr2 of the switch circuits SW that have stored data of "1" are turned ON. Thereby, the gradation voltages on the gradation voltage lines, which are connected to the switch circuits SW with data of "1" stored, of the gradation voltage lines LV1-LVn are applied to the

output lines.

In other words, according to the trigger pulses that start to be fed from time t_0 , the gradation voltages are sequentially fed to the output lines X1-
5 X6, and then fed to the signal lines S1-S6. At time t_1 when the first trigger pulse is generated from the trigger line Q3, the gradation voltages [V2, V3, V4, V2, V1, Vn] corresponding to the image data [2, 3, 4, 2, 1, n] are applied to all the signal lines S1-S6.

10 During the process in which the gradation voltages are applied to the signal lines S1-S6, the scanning circuit 5 sequentially produces the scanning pulses on the scanning lines G1 and G2 at intervals of one-line period. The one-line period is each of the
15 time interval t_0-t_2 and the time interval t_2-t_4 . The scanning line G1 is turned "1" during the one-line period t_0-t_2 , and the scanning line G2 turned "1" during the next one-line period t_2-t_4 .

When the scanning line G1 is "1", the path
20 between the source electrode and the drain electrode in each of the first row pixel TFTs 7 which are connected to the scanning line G1 becomes conductive. Thereby, the gradation voltages from the signal lines S1-S6 are written in the first row pixels 8 during the time
25 interval t_1-t_2 at the latest.

Similarly, during the time interval t_2-t_4 , the gradation voltages [V2, V1, Vn, V4, V3, V1] corresponding to the image data [2, 1, n, 4, 3, 1] are

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In the first method for the application of AC

In this case, the decoders 11 and 12 operate according to the logic shown in Fig. 16. In other words, the outputs out-1 to out-(n/2) and the outputs out-((n/2)+1) to out-n are switched at the odd-numbered field period and the even-numbered field period. Also, in this case, n is twice the gradation number that the image display apparatus can display. If the gradation bit number is 6 bits, the gradation number is 64.

In the second method for the AC voltage

In the second method for the AC voltage

application, the common voltage V_c (the voltage applied to the common electrode 30 shown in Fig. 12) is changed to the AC voltage as shown in Fig. 17. In this case, the voltage range on the gradation voltage line becomes
5 narrow enough to reduce the voltages to the circuits and the power consumption thereon. Here, V_l is the maximum voltage, and the V_n is the minimum voltage. When the high AC voltage value V_{max} is applied to the pixels, the voltage V_l is produced every field period
10 during which the common voltage V_c is the low voltage, and the voltage V_n is produced every field period during which the common voltage V_c is the high voltage, as shown by the line (1). When the AC voltage value V_{max} is applied to the pixels 8, the voltages are
15 applied with the combination opposite to that in the line (1), as shown by the line (2).

When the gradation number is "8" and the gradation voltages are asymmetrical with respect to the input data, the gradation voltages having the
20 characteristics shown in Fig. 18 are selected. In Fig. 18, there are eight different output voltages in each of the odd-numbered fields, and there are eight different output voltages in each of the even-numbered fields. Further, four ones of the output voltages in
25 the odd-numbered fields take the same values as those in the even-numbered fields, so that the four voltages can be used common to the odd-numbered and the even-numbered fields. In other words, when the voltages

On the other hand, when the voltages V1, V5, V8 and V12 are used common to the odd-numbered and the even-numbered fields, only twelve different voltages are enough for the gradation voltages. Thus, the number of the necessary gradation voltage lines is $n=12$. In this case, the decoders 11 and 12 operate according to the logic shown in Fig. 19. For example, in each of the odd-numbered fields, the signal for selecting the voltage V1 is generated for the gradation "1", and the signal for selecting the voltage V5 is generated for the gradation "2". Similarly, the signals for sequentially selecting the voltages V7, V8, V9, V10, V11 and V12 are generated for the gradations "3", "4", "5", "6", "7" and "8".

The gradation number may be arbitrary, and the necessary number of the different voltages (namely, the number n of the gradation voltage lines) depends on the number of the voltages that can be used common to the odd-numbered and the even-numbered fields. The maximum number is twice the gradation number, and the minimum number is equal to the gradation number.

Fig. 20 shows an example of the circuit layout of the DA converter 4. This example illustrates only the region including two switch circuits SW in the lateral direction, and four switch circuits SW in the longitudinal direction with respect to the drawing

sheet. The gradation voltage lines LV1 and LV2, and the switch drive lines D1-1, D1-2, D2-1 and D2-2 are the metal wiring lines formed as the same layer to run in the lateral direction with respect to the drawing sheet. The switch drive lines transmit the fast signals, and the gradation voltage lines are grounded on the AC basis. However, since the length of the wiring line is required to be long in the lateral direction, the switch drive lines and the gradation voltage lines that are formed in the lateral direction are made of preferably aluminum or copper in order to reduce their resistance. The trigger lines Q1 and Q2 and the output lines X1-X4 are made of the metal wiring lines formed as the same layer as the metal wiring lines forming the gates of the TFTs, and are formed in the longitudinal direction to intersect the gradation voltage lines and the switch drive lines. The switch circuits SW are formed in each of the spaces between the switch drive line D1-1 and the gradation voltage line LV1, between the gradation voltage line LV1 and the switch drive line D1-2, between the switch drive line D2-1 and the gradation voltage line LV2, and between the gradation voltage line LV2 and the switch drive line D2-2. In each of the switch circuits SW, two n-channel TFTs tr1 and tr2 are formed, and are connected by the metal wiring lines and the gate metal film according to the circuit diagram shown in Fig. 4. The TFTs tr1 and tr2 are formed at the intersections of

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According to this embodiment, even when the image display apparatus is of the multi-tone display type, the number of the wiring lines in the

In addition, even when the gradation bit number is "6", the number of the transistors of the DA converter 4 per signal line can be made as small as $2 \times 64 = 125$. The width of the DA converter 4 in the longitudinal direction with respect to the drawing sheet is $52 \mu\text{m} \times 64 = 3.584 \text{ mm}$, and thus the area to be occupied by the non-display region of the image display apparatus can be reduced.

Each switch drive line has three intersections 41-43 shown in Fig. 20 with the longitudinal lines including two signal lines, or 1.5 intersections occur per signal line. That is, the wiring lines that intersect are only two output lines

and one trigger line. In addition, since two switch drive lines are provided in parallel on both sides of each gradation voltage line, the switch drive lines never intersect each other. Therefore, the number of the intersections between the wiring lines is constant
5 irrespective of the increase of the gradation number n . Accordingly, even though the image display apparatus display is of the multi-tone display type, the number of the intersections (i.e., the intersection
10 capacitance) can be reduced, so that it is possible to reduce the power consumption due to the transmission of the fast signals on the switch drive lines.

Moreover, according to this embodiment, the number of the state changes in n switch drive lines
15 connected to each of the decoders 11 and 12 is maximum "2", and $2 \times (1 - (1/n))$ in average. Here, $1/n$ indicates the probability at which the same data occurs.

According to this embodiment, the maximum change of the gradation bit number is two or more, and
20 the average bit value is four or more, thus the number of the changes being small. In other words, since each of the decoders 11 and 12 produces the signal of "1" on the single switch drive line alone, the number of the data change times can be reduced.

25 Therefore, as compared with the conventional system in which the multi-tone data is inputted as the binary data via the data bus, this embodiment can reduce the power consumption to the maximum value of 2

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The switch circuit SL includes n-channel TFTs tr3-tr6, and a condenser (electrostatic capacity) C1. This switch circuit SL has a function to serve as switching means for selecting a specified gradation voltage line in response to the trigger signal and data (switch drive signal) from the switch drive line, and also a function to serve as a level shifter (voltage level conversion means) for amplifying the voltage on the switch drive line. The gate electrodes of the TFTs tr3 and tr5 are connected to the trigger line Q1. When the trigger pulse (trigger signal) is fed via the trigger line Q1, those TFTs sample the voltages on the switch drive line D1 and the ground line GND in synchronism with this trigger pulse so that those voltages can be applied to the ends a and b of the condenser C1, respectively. The opposite ends of the condenser C1 are connected to the gate and drain electrodes of the TFT tr4, respectively. The voltage at the end b of the condenser C1 is shifted in level by the pulse on the pulse line LP.

The source and drain electrodes of the TFT tr6 are connected to the gradation voltage line LV1 and the output line X1, respectively. The TFT tr6 can serve as a switch that is controlled in its ON/OFF state by the voltage at the end b of the condenser C1 so as to connect or disconnect the gradation voltage line LV1 and the output line X1. In other words, the TFT tr6 is turned ON (conductive) when the high voltage

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5 drive lines D1-Dn are similarly constructed as above.

10 voltage produced by sampling the switch drive line D1
appears at the point a, and the voltage of 0 V produced
by sampling the ground line GND appears at the point b,
as described above. The logic on the switch drive line
is "1" or "0", and the voltage of "1" is the voltage
15 Vsig that is smaller than VDD but larger than at least
the threshold voltage of the TFT tr3. This voltage
Ssig is usually smaller than 3 V. Therefore, when the
voltage on the switch drive line is "1", the voltage on
the switch drive line is sampled so that the voltage at
20 the point a is Vsig. When the voltage on the switch
drive line is "0", the voltage on the switch drive line
is sampled so that the voltage at the point a is 0 V.
After the completion of sampling, the pulse of voltage
VDD is applied on the pulse line LP. Here, when the
25 voltage at the point a is Vsig, the TFT tr4 is turned
ON, and thus the voltage at the point b increases. The
voltage at the point a is also risen through the
condenser C1, and further the increase of the voltage

5 OFF, and thus the voltage at the point b remains 0 V.

10 switched ON/OFF to control the wider range of the
voltage on the gradation voltage line.

20 decoding, the signal of "1" is produced on one of the switch drive lines D1-Dn, and the signal of "0" on the other switch drive lines. When the shift register 2 sequentially produces the trigger pulses on the trigger lines Q1-Q3 in synchronism with the inputting of this
25 image data, the TFTs tr3 and the TFTs tr5 connected to the trigger lines Q1-Q3 are turned ON. Of the switch circuits SL, data of "1" is stored in the switch circuits SL connected to the switch drive line on which

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is "1", the pixel TFTs 57 connected to the scanning line G1 have their source-drain paths made conductive, so that the gradation voltages from the signal lines S1-S3 are written in the first row of pixels 58 by time
5 t2 at the latest.

Similarly, during one-line period of time t2-t4, the gradation voltages [V2, Vn, V3] corresponding to the image data [2, n, 3] are supplied to all the signal lines S1-S3 in the time period t3-t4, and the
10 gradation voltages from the signal lines S1-S3 are written in the second row of the pixels 58 by time t4 at the latest. By the repetition of the above operations, it is possible to apply the aimed voltages to all the pixels 58 in the display region 56, thus
15 displaying the image.

When the image display apparatus according to this embodiment is driven, the drive frequency of the decoder 53 is the same as the frequency of the image data inputted via the data line Data. The switch
20 circuits SL are once driven by the trigger pulses from the trigger lines during one line period. In addition, since at least two data are inputted during one line period, the drive frequency of the decoder 53 is twice that of the switch circuits SL or more.

25 When the image display apparatus according to this embodiment is used as the liquid crystal display apparatus, the AC voltage with the polarities inverted every field is applied to each of the pixels 58. The

5 employed.

Fig. 24 shows an example of the circuit layout of the DA converter 54 in this embodiment. This example illustrates only the region including two switch circuits SL in the lateral direction and two switch circuits in the longitudinal direction with respect to the drawing sheet. The gradation voltage lines LV1 and LV2, the switch drive lines D1 and D2, the ground lines GND, and the pulse lines LP are made of the metal wiring lines as the same layer, and are formed in the lateral direction. The fast signals are transmitted on the switch drive lines, and the gradation voltage lines are grounded on the AC basis. Since the wiring lines are necessary to be long in the lateral direction with respect to the drawing sheet, the wiring lines in the lateral direction are made of preferably aluminum or copper in order to have low resistance. The trigger lines Q1 and Q2 and the output lines X1 and X2 are made of the metal wiring lines formed as the same layer as those forming the gates of the TFTs, and are arranged in the longitudinal direction to intersect the gradation voltage lines and the switch drive lines. The switch circuits SL are formed in each of the spaces between the switch drive

In addition, the number of the intersections of the switch drive lines in this embodiment is "2" per signal line, as shown at intersections 44 and 45 in Fig. 24. The wiring lines that intersect are two output lines and one trigger line. Moreover, since two switch drive lines are provided in parallel on both sides of each gradation voltage line, respectively, the switch drive lines never intersect each other.

Also, when the numbers of the power supply lines and the common signal lines such as the ground lines GND and the pulse lines LP are increased, those lines can be arranged in parallel with the switch drive lines. Thus, the number of the intersections of the switch drive lines are never increased. Therefore, the number of the lines intersected is unchanged even when the gradation number n is increased. Thus, even when the image display apparatus is of the multi-tone

display type, the lines intersected, or the intersection line capacitance can be decreased. As a result, it is possible to reduce the power consumption on the switch drive lines on which the fast signals are transmitted.

Moreover, according to this embodiment, the number of the data change times on the n switch drive lines connected to one single decoder 53 is maximum "2", and $2 \times (1 - (1/n))$ in average. That is, in this embodiment, the maximum gradation bit number is two or more, and the average gradation bit number is four or more, thus the number of changes being small.

As compared with the conventional system in which the multi-tone image data is inputted as the binary data via the data bus, the maximum power consumption is 2 bits or more, and the average power consumption is 4 bits or more in this embodiment. Accordingly, it is possible to reduce the power consumption even when the multi-tone image is displayed.

In addition, when the decoder 53 is constructed as the external IC 23, the power consumption due to the drive of the parasitic capacitance of the flexible cable via which the external IC 23 and the image display apparatus are connected can be reduced. Accordingly, it is possible to reduce the power consumption of the fast signals on the external wiring line such as a flexible cable.

5 lines can be decreased. Thus, it is possible to reduce the power consumption on the switch drive lines.

10 shift register 2, decoders 64 and 65 in place of the
decoder 3, and a DA converter 66 in place of the DA
converter 4 are formed in the non-display region of an
insulating substrate 61. The constructions of the
other portions are the same as in Fig. 1. In this
15 embodiment, only the arrangement concerned with the
signal lines S1-S4 is described.

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20  produce the trigger pulses on the trigger lines Q1, Q2,
    Q3 and Q4 in synchronism with the image data input.

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25 data, data of "1" is produced on one of the switch drive lines D1-1 to Dn-1 or D1-2 to Dn-2, and data of "0" is produced on the other switch drive lines. The decoders 64 and 65 are disposed to oppose each other

with the DA converter 66 interposed between them. Each of the decoder 64 and 65 may be constructed as the external IC 23 as shown in Fig. 7.

The DA converter 66 has n gradation voltage lines LV1-LVn, 2 × n switch drive lines D1-1 to Dn-1 and D1-2 to Dn-2, trigger lines Q1-Q4, and output lines X1-X4. The switch drive lines D1-1 to Dn-1 are connected to the output ends of the decoder 64. The switch drive lines D1-2 to Dn-2 are connected to the output ends of the decoder 65. The trigger lines Q1-Q4 are connected to the output ends of the shift registers 62 and 63. The output lines X1-X4 are connected to the signal lines S1-S4.

The switch drive lines D1-1 to Dn-1 and D1-2 to Dn-2 are arranged in parallel with the gradation voltage lines LV1-LVn. The trigger lines Q1-Q4 and the output lines X1-X4 are arranged to intersect the switch drive lines D1-1 to Dn-1 and D1-2 to Dn-2. The switch circuits SW are formed in the regions near the intersections of the wiring lines. The different voltages V1-Vn are applied on the gradation voltage lines LV1-LVn as the gradation voltages corresponding to the display gradations.

The switch circuit SW is constructed of the n-channel TFTs tr1 and tr2, and the condenser Cm, like the first embodiment. However, the switch circuits SW connected to the output lines X1 and X2 are connected to the switch drive lines D1-1 to Dn-1. The switch

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circuits SW connected to the output lines X3 and X4 are connected to the switch drive lines D1-2 to Dn-2.

In this embodiment, the switch drive lines are divided into two separate regions, but the
5 gradation voltage lines are used common to the two regions. Therefore, the image can be prevented from being irregular due to the very small differences between the gradation voltages. The switch drive lines may be divided into more than two regions.

10 The circuits of the image display apparatus are operated as shown in Fig. 26 to display the image on the display region 68. As the multi-tone image data, the left and right halves of the image are fed to the input end of the decoders 64 and 65 via the data
15 lines Data-1 and Data-2, respectively. When the image data #1-#4 of the first row to be displayed are [2, 4, 3, 2] from left to right in turn, image data of [2, 4] and image data of [3, 2] are fed via the data lines Data-1 and Data-2, respectively. These data are
20 decoded by the decoders 64 and 65, respectively. According to the logic of the decoding, one of the switch drive lines D1-1 to Dn-1 and one of the switch drive lines D1-2 to Dn-2 are turned "1", and the other lines are turned "0".

25 At this time, the trigger pulses are supplied from the shift registers 62 and 63 to the trigger lines Q1 and Q2 and the trigger lines Q3 and Q4 in synchronism with the inputting of the image data. When

the trigger pulses are sequentially fed to the trigger lines, data of "1" is stored in the switch circuits SW connected to the switch drive lines of "1", of the switch circuits SW to which the trigger pulses are applied. On the other hand, data of "0" is stored in all of the other switch circuits connected to the switch drive lines of "0". These stored data are held until they are again sampled. During this interval, the TFTs tr2 of the switch circuits SW in which "1" is stored are turned ON. As a result, the gradation voltages on the gradation voltage lines connected to the switch circuits SW in which "1" is stored, of the gradation voltage lines LV1-LVn, are supplied to the corresponding output lines.

15 In other words, the gradation voltages are sequentially fed to the output lines X1-X4 according to the trigger pulses generated from time t0, and are supplied to the signal lines S1-S4. At time t1 at which the final trigger pulses are fed to the trigger lines Q2 and Q4 and the generation of the trigger pulses ends, the gradation voltages [V2, V4, V3, V2] corresponding to the image data [2, 4, 3, 2] are fed to all the signal lines S1-S4.

In the process in which the gradation voltages are fed to the signal lines, the scanning pulses are sequentially produced from the scanning circuit 67 to the scanning lines G1 and G2 every line period. One-line period is each of the time periods

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Therefore, since at least two data are fed in each line period, the drive frequency of the decoders 64 and 65 is twice that of the switch circuits SW, or more.

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gradations. Thus, when the layout rule is 4- μ m spacing and 4- μ m line width, the space necessary for the wiring is only $(4+4) \times 2 = 16 \mu$ m in width, which is smaller than 42 μ m, for example. Therefore, this embodiment
5 can display the image with the high definition over 200 pixels/inch.

Moreover, the number of the intersections of the switch drive lines in this embodiment is two per signal line, like in the second embodiment. The
10 intersection wiring lines are two output lines and one trigger line only. Since two switch drive lines are provided in parallel on both sides of the gradation voltage line, the switch drive lines never intersect each other. Therefore, the number of the intersection
15 wiring lines is constant irrespective of the increase of the gradation number n. Thus, even when the image display apparatus is of the multi-tone display type, the intersection lines (i.e., the intersection wiring capacitance) becomes small, so that it is possible to
20 reduce the power consumption on the switch drive lines on which the fast signals are transmitted.

In addition, according to this embodiment, the number of the data changes (the number of the state changes) on n switch drive lines connected to each of
25 the decoder 64 and 65 is maximum "2", and the average value thereof is $2 \times (1 - (1/n))$. In other words, according to this embodiment, the maximum gradation bit number is two or more, and the average gradation bit

Therefore, as compared with the conventional system in which the multi-tone data is inputted as the binary data via the data bus, the maximum power consumption is 2 bits or more and the average power consumption is 4 bits or more according to this embodiment. Therefore, it is possible to reduce the power consumption even in the image display apparatus which displays the multi-tone image.

Also, when the decoders 64 and 65 are constructed as the external IC 23, the power consumed when the parasitic capacitance of the flexible cable connecting the external IC and the image display apparatus is driven can also be reduced. Thus, it is possible to reduce the power consumption when the fast signal is transmitted on the external line such as a flexible cable.